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DIGITAL DEVICES INC.

200 MICHAEL DRIVE • SYOSSET, NEW YORK 11791

January 1, 1967

The CRT Refresher which you inquired about is a single delay line version of the Display Buffer shown on the attached data sheet. Individual lines are available with or without electronics in 5 standard case sizes.

Type #	Length	Width	Thickness	Max. Delay	Max. Storage
705	7"	6"	1/2"	3,000 us	6,000 bits
706-1	10 1/2"	9 1/2"	5/8"	5,000 us	8,000 bits
706-2	10 1/2"	9 1/2"	1"	10,000 us	14,000 bits
707-1	11 1/2"	10 1/2"	1/2"	4,500 us	9,000 bits
707-2	11 1/2"	10 1/2"	1"	11,000 us	18,000 bits

Many special case sizes are also available.

Electronic packages are available to interface to RTL, TTL, DTL, Sylvania SUHL, MECL, or Signetics Utilogic, as well as conventional NPN and PNP logic levels. Power supplies required are ± 12 volts and $+V_{CC}$.

Prices start at $200 per delay line, $400 with electronics in small quantities, and go as low as 1/2¢ per bit for the delay line, 1¢ per bit with electronics.

Delivery is 6 to 8 weeks after receipt of order.

We are ready to supply further details on either delay lines or circuitry packages as you may require. Please contact us or our representative if we may be of any further assistance.

P. A. Bauer

Paul A. Bauer
Sales Manager

Product Specification

MODEL 528E 1000

DISPLAY BUFFER

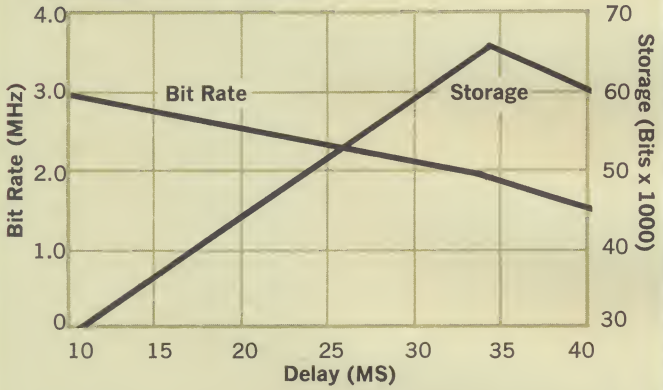
Modular memory for flicker-free refreshing of digital tv display systems is offered by the DDI Model 528E-1000 Display Buffer.

FEATURES

Low Cost—as low as 1½¢ per bit
High Reliability—no moving parts; nothing to wear out
Low Power—less than 10 watts from common dc voltages
Large Capacity—standard package stores 67,728 bits
High Speed—to 3 MHz; faster with multiplexing
Expandable—16,000 bit modules may be added indefinitely
Compatible—supplied with system interface electronics
Rugged—housed in cast aluminum o-ring sealed case
Stability—can be synchronized to stable system clock

DDI Display Buffer stores 67,728 bits in four sealed delay lines complete with electronics. Separate interface circuit board matches any IC or discrete logic levels.

PERFORMANCE RANGE



ELECTRICAL CHARACTERISTICS

Maximum Storage—67,728 bits
Bit Rate—3 MHz max., 2 MHz typical
Unit Delay—45 msec max., 33 msec nominal
Delay Adjustment—±8 us
Adjustment resolution—±.025 us
Circuitry—includes driver, amplifier, detector, retiming, and interface
System Inputs
Logic—NRZ data
Interface—TTL, MECL, DTL, RTL, or NPN or PNP discrete circuit levels
Clock
Frequency—up to 3 MHz
Stability—1 ppm total
Duty cycle—50% nominal
Jitter (input data to clock)—20 ns maximum

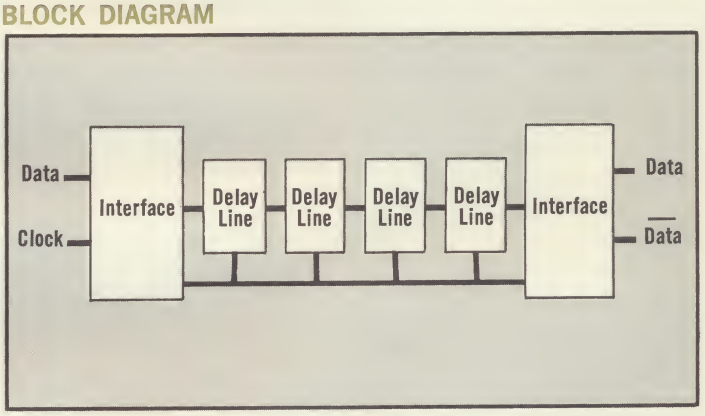
Power

Voltage	+12V	−12V	+Vcc
Regulation	±2%	±2%	±5%
Current	440 ma	200 ma	100 ma

System Outputs
Logic—NRZ and NRZ Complement Data
Interface—same as input

Display buffer unit contains 4 o-ring sealed, cast case delay lines, each delay line storing up to 16,672 bits and containing its own read and write electronics. A separate interface board matches package electronics to any system level desired. Total package storage of 67,728 bits, and refresh rates of 25 cps to over 50 cps are available.

BLOCK DIAGRAM



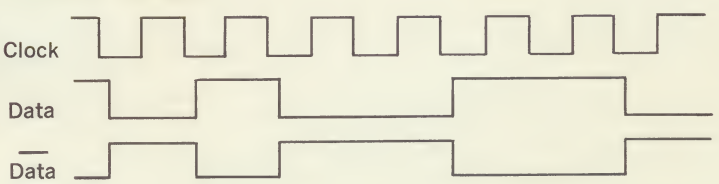
MECHANICAL CHARACTERISTICS

Dimensions—16½" x 14" x 3½"
Connector—Microdot Receptacle #SOS-93/P/N 31-47 or equivalent
Mounting—bolts to relay rack panel
Outline drawing—DDI #528E-1000-000

INPUT TIMING

Any phasing between clock and data is permissible so long as jitter requirement is met.

OUTPUT TIMING



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7850 Printed in U.S.A. 12/66